

METHOD FOR DETECTING RESISTIVE-OPEN DEFECTS
IN SEMICONDUCTOR MEMORIES

This application claims priority of provisional patent application titled, "A New Efficient Solution to Cover Resistive-Open Defects for Semiconductor Memories," (S/N 60/556,706) filed on March 26, 2004 and is incorporated by reference in its entirety.

The present invention relates to the field of testing of semiconductor memories and
5 in particular, to a method for resistive-open defects in semiconductor memories.

Systematic and automatic testing of integrated circuits becomes increasingly important. With each new generation of integrated circuits component density, number of system functionalities, and clock speed are substantially increased. Integrated circuits have reached such complexity and speed that process defects are no longer detectable using even
10 the most exhaustive and expensive conventional testing procedures. However, customers will not accept products that show their hidden defects in operational use, thereby rendering, for example, life support systems or aircraft control systems unreliable.

At the present time, embedded semiconductor memories are operating at high speed with clock cycles reaching 2 ns for SRAMS, or even less for the new generation of CMOS
15 whose critical dimensions are on the order of 90 nanometers. Testing of the embedded semiconductor memories is generally performed by Built-In-Self-Test (BIST) or a tester using scan test mode. In the BIST – or the tester – consecutive test patterns are generated to perform read and write operations at the memory, according to a predetermined March test. The march test is well known in the art and is often considered a sufficient test for
20 semiconductor memories.

Resistive open defects not only cause static faulty behavior of the semiconductor memory, which is easily detected, but also dynamic faulty behavior known as "slow to rise" and "slow to fall" either in the data path or the address path. Depending on the resistance of the defect - defect size – the delays vary considerably. Big delays resulting in static faulty
25 behavior are easily detected. The detection of small delays corresponding to small sized defects requires high speed testing using the BIST or scan test. Ideally, the semiconductor memories need to be tested at their operating frequency. If a semiconductor memory is not tested at the operating frequency, small sized resistive open defects are not detected even with the correct test patterns applied. However, a high speed BIST is not easily
30 incorporated into the memory layout, because of the delay needed for the output analyzer of the BIST, the extra time needed for the synthesis, and the additional area needed for the

high speed BIST. Increasing the speed of the BIST implies a substantial increase in area for the BIST, which is unacceptable for most applications. Furthermore, testing embedded semiconductor memories using scan test mode needs additional test time due to scan-in and scan-out of the data, which is done in series, and, therefore, substantially increases the test
5 time for big memories with a high number of pins.

As modern fabrication process change from aluminum-based interconnect to a copper-based interconnect, resistive-open defects are becoming the dominant defects. For example, in an aluminum process, resistive metal bridging is more prevalent than resistive opens. In contrast, in a copper process, resistive opens are more prevalent.

10 However, as outlined above, testing at frequencies below the operating frequency of a semiconductor memory may result in undetected delay faults such as those manifested by resistive open defects, resistive bridges, and capacitive coupling.

There is a need to provide a method for reliably detecting delay faults in new generation semiconductor memories using a BIST or tester operating at a lower frequency
15 than the operating frequency of the semiconductor memory.

The present invention has been found useful in detecting resistive-open defects in semiconductor memories. These resistive-open defects manifest themselves as delay faults leading to slow-to-rise and slow-to-fall behavior at the memory address decoder, the pre-charge circuits, the write data lines, the global inputs/outputs, and also in the memory cell
20 matrix.

Through the use of a BIST (built-in-self-test) or a test operating at lower frequencies than the operating frequency of the semiconductor memory, the invention provides a reliable method for detecting these delay faults.

In an embodiment according to the present invention, there is a method for
25 detecting delay faults in a semiconductor memory. The method comprises generating address bits and data bits according to a test pattern suitable for testing the semiconductor memory. The address bits and data bits are validated. The address bits and data bits are provided to input ports of the semiconductor memory. In dependence upon the address bits, memory operation is started, wherein a time interval between the provision of the address
30 bits and the data bits and the start of the memory operation is approximately equal to an operating clock cycle of the semiconductor memory.

In another embodiment according to the present invention there is further provided a method for detecting delay faults in a semiconductor memory. The method comprises

generating address bits and data bits according to a test pattern suitable for testing the semiconductor memory. The address bits and data bits are validated. The address bits and the data bits are provided to the input ports of the semiconductor memory. In dependence upon the address, wherein a time interval between the provision of the address bits and the data bits and start of the write operation is approximately equal to an operating clock cycle of the semiconductor memory, the data bits are written into the semiconductor memory. According the test pattern, a second address bits are generated. The second address bits are validated. In dependence upon the second address bits, wherein a time interval between the provision of the address bits and start of the read operation is approximately equal to an operating clock cycle of the semiconductor memory, the second data bits out of semiconductor memory are read. The second data bits are compared with predetermined data to obtain a comparison result and if the comparison result is indicative of a match indicating that the operation was fault free.

In yet another embodiment according to the present invention there is provided a test circuitry for detecting delay faults in a semiconductor memory comprising address and data generating circuitry for generating address bits and data bits according to a test pattern suitable for testing the semiconductor memory. There is validation circuitry for validating the address bits and the data bits. Connecting circuitry in communication with the semiconductor memory for provides the address bits and the data bits to the semiconductor memory. Timing circuitry for provides a time signal for timing the provision of the address bits and the data bits and start of the memory operation such that a time interval between the provision of the address bits and the data bits and the start of the memory operation is approximately equal to an operating clock cycle of the semiconductor memory.

The above summaries of the present invention are not intended to represent each disclosed embodiment, or every aspect, of the present invention. Other aspects and example embodiments are provided in the figures and the detailed description that follows.

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 is a flowchart of testing of the memory according to an embodiment of the present invention;

FIG. 2 is a diagram schematically illustrating address and data set-up time in a BIST;

FIG. 3 is a diagram schematically illustrating simulation results of a semiconductor memory test;

FIG. 4 is a diagram schematically illustrating simulation results of a semiconductor test with an injected open defect at the least significant bit of the X address decoder;

5 FIG. 5 is a diagram schematically illustrating an enlarged portion of the diagram shown in FIG. 4; and

FIG. 6 is a diagram schematically illustrating simulation results of a semiconductor test using the method according to the invention.

10 In the following the invention will be described in connection with the BIST for simplicity. As will become evident, the invention also may be implemented using a tester in scan test mode.

The frequency of the BIST has a significant impact on the delay fault detection. High speed testing increases detection of delay faults by detecting small delay faults caused, for example, by resistive open defects. However, implementation of the BIST at high testing
15 frequency is not feasible in most applications.

The BIST generates data with corresponding addresses and runs consecutive write and read operations in increasing and decreasing address order. In case of read operation, an output analyzer of the BIST compares the read out data with predetermined logic values. If the read out data match the logic values, the memory is fault free, otherwise, the memory
20 is faulty. Refer to FIG. 2. FIG. 2 illustrates the wave forms of the data and address generation 221, 231 in relation to a signal provided by a test clock CL. Address and data set-up time are defined as the time between address generation (222, 223) and data generation (232, 233) and a positive edge of the test clock CL.

The process steps 100 of the BIST are shown in FIG. 1. Depending upon the march
25 test, the BIST generates the address and data backgrounds 110. The BIST holds the state of the memory in order for the data bits and the address bits to become valid 120. The address and data background are delivered to the memory inputs 130. Using a positive/negative edge of the test clock, memory operation is begun 140. The memory operation may either be a read or a write. Depending upon the write enable signal, the data background is either
30 written to the memory or is read out from the memory 160. The read out data is compared with predetermined logic values 170.

The above steps are repeated depending on the complexity of the test patterns and the memory size. The end of testing is reported by the BIST when a ready signal is delivered together with a second flag indicating the tested device being fault free or faulty.

FIG. 2 shows the waveforms of the address generation 230 and data generation 220 with the memory clock (CL) 210. The setup time 225, 235 for the address and data is the time (which includes a hold time 222, 232 and data valid interval 223, 233) that exists between the address and data background generation (221, 231) and the positive/negative edge of the clock.

Generally, the address and data generation is performed at a lower frequency than the operating frequency of present semiconductor memories. Thus, delay faults are masked when the test patterns – address bits and data bits – are delivered to the memory inputs for a relatively long time before the start of the memory operation – positive/negative edge of the clock signal. A BIST operating at 50 MHz needs 20 ns for generating address bits and data bits, and data comparison for the output analyzer in case of a read operation. Therefore, approximately 10 ns are needed to generate and deliver a set of address bits and data bits to the memory inputs. For example, a semiconductor memory is operating at 2 ns clock cycle, if the address bits and data bits are delivered to the memory approximately 10 ns before the positive/negative edge of the clock signal, the periphery circuitry of the memory is already in a substantially stable state before the positive/negative edge of the clock signal. Therefore, a delay fault caused by a defect in the memory periphery is not detected during application of the test pattern due to a delay of 10 ns before the positive/negative edge of the clock signal masking the delay fault.

Nowadays, the memories are self-timed, i.e. an internal clock for controlling the read/write operation is generated based on the positive/negative edge of an external clock signal. The self-timing techniques avoid incomplete read/write operations to occur. For testing delay faults, the state of the memory circuit before the positive/negative edge of the internal clock is critical. Small delay faults are detected when the state of the memory circuit is not yet stable due to the delay fault. When the positive/negative edge of the external clock signal is on time, the internal clock signal of the memory is generated and the memory circuit is still not yet stable. Thus, the delay fault has an impact on the memory behavior and is detected. Therefore, the time interval separating the positive/negative clock edge and the delivery of the memory inputs is critical. When the time interval between the provision of the address bits and data bits and the positive/negative clock edge is large

compared to the memory clock cycle then address decoder, write circuitry, sense amplifiers, pre-charge and discharge circuitry are already stable before the positive/negative clock edge initiates the read/write operation.

Referring to FIG. 3, a simulation result 300 of a march test of a memory with six
5 output 320 pins $q[0, \dots, 5]$ is shown. The memory operates at 2 ns clock cycle, while the BIST performs the March test at 50 MHz – 20 ns clock cycle. Thus the address and data set-up time is approximately 10 ns. The output pins 320 and the clock 310 are plotted.

FIG. 4 illustrates the simulation results 400 performed under same conditions with
an injected open defect at the least significant bit of the X address decoder. This open
10 defect results in a slow-to-rise fault indicated in the waveform 415 of the $V(a_2_open)$ diagram. The slow-to-rise fault 425 is more clearly visible in the enlarged section shown in FIG. 5. The pin $a_2_$ reaches 410 the logic value of one with a delay of 5 ns, while the memory operates at 2 ns clock cycle. However, this defect is not detected when the BIST is operated at a frequency lower than the operating frequency of the semiconductor memory.
15 Referring to FIG. 5, the slow-to-rise fault 425 is zoomed in the plot 500, pin $a_2_$ (510) is a pin without resistive defects. Pin a_2_open (520) reaches a logic-one 5ns later.

In a method for detecting delay faults in semiconductor memories according to an embodiment of the present invention, the time between the delivery of the address bits and the data bits to the memory inputs and the start of the memory operation is reduced either
20 by shifting the positive/negative clock edge or the address and data validation in order to detect delay faults.

In another method for detecting delay faults in semiconductor memories according to the present invention data bits and address bits are generated depending on a test pattern such as a march test. The address bits and data bits are then validated. After the validation
25 the address bits and data bits are then delivered to the memory inputs. The positive/negative edge of the test clock starts memory operation – read or write - depending on a write enable signal. The delivery of the address bits and data bits and the start of the memory operation are timed such that a time interval therebetween is approximately equal to an operating clock cycle of the semiconductor memory. The appropriate time interval is
30 obtained by appropriate timing of the address and data validation or, alternatively, by appropriate timing of the positive/negative edge of the test clock. In case of a read memory operation the data bits are read out of the memory and compared with predetermined logic values. The above steps are repeated by generating data bits and address bits and running

consecutive write and read operations in, for example, increasing or decreasing address order. In case of a delay fault free memory the read out data bits match the predetermined values; otherwise if, for example, one data bit does not match the predetermined value, the memory is determined to be faulty.

5 The above method for detecting delay faults in semiconductor memories is highly advantageous, enabling delay fault detection using a BIST operating at a frequency below the operating frequency of the semiconductor memory. For instance, a semiconductor memory operating at 200 MHz needs to be tested at the same frequency or smaller delay faults are not detected. Testing the semiconductor memory at 50 MHz or even 150 MHz
10 using a conventional BIST does not enable detection of small delay faults. By timing the delivery of the address bits and data bits and the start of the memory operation such that the time interval therebetween is approximately equal to the operating clock cycle of the semiconductor memory, both the address decoder and the read/write circuitry are stressed in time appropriately, enabling detection of small delay faults. Furthermore, the method
15 according to the invention is also applicable for testing self-timed semiconductor memories using the positive/negative edge of the internal memory clock signal.

 This obviates a need for operation of the BIST at the operating frequency of the memory, substantially reducing the BIST area of a memory chip. In an embodiment the BIST is implemented such that it is operating at a maximum possible frequency – maximum
20 possible trade off area – and the frequency gap between the BIST frequency and the operating frequency of the memory is then compensated by appropriate timing of the delivery of the address bits and data bits and the start of the memory operation.

 FIG. 6 illustrates a simulation similar to that of FIG. 4 with the timing arranged according to an embodiment of the present invention. The simulation 600 shows that the
25 delay fault is detected when the appropriate timing of the delivery of the address bits and data bits and the start of the memory operation is applied. The memory outputs q_1 and q_2 provide unexpected logic values 620 at 50 ns, while all memory outputs provide incorrect logic values 630 at 240 ns.

 The method according to the invention is easily implemented in conventional BIST
30 circuitry or tester circuitry enabling operation of the BIST or the tester at a lower frequency than the operating frequency of the memory under test while enabling detection of small delay faults.

Numerous other embodiments of the invention will be apparent to persons skilled in the art without departing from the spirit and scope of the invention as defined in the appended claims.